# Embedded Systems Design

Embedded Hardware 3

EMBD21000-14-ILT (v1.0H)

**Course Specification**

## Course Description

The Xilinx Zynq™ Extensible Processing Platform (EPP) provides a new level of system design capabilities. This course brings experienced FPGA designers up to speed on developing embedded systems using the Embedded Development Kit (EDK). The features and capabilities of the Zynq EPP as well as concepts, tools, and techniques are included in the lectures and labs. The hands-on labs provide students with experience designing, expanding, and modifying an embedded system, including adding and simulating a custom AXI-based peripheral.

Additionally, the features and capabilities of the Xilinx MicroBlaze™ soft processor are also included in the lectures and labs.

**Level** – Embedded Hardware 3

**Course Duration** – 2 days

**Price** – $1500 or 15 Training Credits

**Course Part Number** – EMBD21000-14-ILT

**Who Should Attend?** – Engineers who are interested in developing embedded systems with the Xilinx Zynq EPP or MicroBlaze soft processor core using the Embedded Development Kit

**Prerequisites**

- FPGA design experience
- Completion of the *Essentials of FPGA Design* course or equivalent knowledge of Xilinx ISE® software implementation tools
- Basic understanding of C programming
- Basic understanding of microprocessors
- Some HDL modeling experience

**Software Tools**

- Xilinx ISE Design Suite: Embedded or System Edition 14.1

**Hardware**

- Architecture: Zynq-7000 EPP and 7 series, Spartan®-6, and Virtex-6 FPGAs*
- Demo board: Zynq-7000 EPP ZC702 or Spartan-6 FPGA SP605*

* This course focuses on the Zynq-EPP, 7 series, Spartan-6, and Virtex-6 FPGA architectures. Check Hardent for the specifics of the in-class lab board or other customizations.

After completing this comprehensive training, you will have the necessary skills to:

- Describe the various tools that encompass the Xilinx Embedded Development Kit (EDK)
- Rapidly architect an embedded system containing a MicroBlaze™ or Cortex™-A9 processor by using the Base System Builder (BSB) or PS Configuration Wizard
- Utilize the Eclipse-based Software Development Kit (SDK) to develop software applications and debug software
- Create and integrate your own IP into the embedded processing environment
- Simulate your custom AXI interface-based peripheral by using a Bus Functional Model (BFM)

## Course Outline

**Day 1**

- EDK Overview
- Base System Builder and the Processing System Configuration Wizard
- **Lab 1:** Hardware Construction with the Base System Builder or Processing System Configuration Wizard
- Software Development Using SDK
- **Lab 2:** Adding and Downloading Software
- Introduction to AXI
- Interrupts
- Adding Hardware to an Embedded Design
- **Lab 3:** Adding IP to a Hardware Design

**Day 2**

- MicroBlaze Processor Basics
- Cortex-A9 Processor Basics
- Designing Your Own AXI Peripheral Using the IPIC Interface
- Adding Your Own Peripheral to the IP Catalog
- **Lab 4:** Building Custom AXI IP for an Embedded System
- Bus Functional Model Simulation
- **Lab 5:** BFM Simulation
- Adding Your Own IP to the Embedded System
- **Lab 6:** Integrating a Custom Peripheral

## Lab Descriptions

- **Lab 1:** Hardware Construction with the Base System Builder (Microblaze Processor) or Processing System Configuration Wizard (Zynq EPP) – Create an XPS project by using a wizard to develop a basic hardware system and generate a series of netlists for the embedded design.
- **Lab 2:** Adding and Downloading Software – Complete the processes begun in Lab 1 using the SDK tools to create a software BSP and sample application. Configure the device and download the application.
- **Lab 3:** Adding IP to a Hardware Design – Add IP to an existing processing system using the System Assembly View in Xilinx Platform Studio. Configure the device and download the application
- **Lab 4:** Building Custom AXI IP for an Embedded System – Create and add a custom AXI peripheral (LCD interface) to your design by using the Create and Import Peripheral Wizard.
- **Lab 5:** BFM Simulation – Use the ISim simulator to perform Bus Functional Model simulation to verify functionality of the LCD bus peripheral added in the preceding lab.
- **Lab 6:** Integrating a Custom Peripheral – Put it all together: add custom IP to the design project, then integrate the processor sub-system with other logic in an ISE software design project.

## Register Today

Hardent, the Authorized Training Provider (ATP) for Canada (excluding British Columbia), New England (Connecticut, Maine, Massachusetts, New Hampshire, Rhode Island and Vermont) and the Southeastern United States (Alabama, Florida, Georgia, Mississippi, North Carolina, South Carolina and Tennessee) delivers Xilinx public and private courses in your region. Visit www.hardent.com/training or contact Hardent's Training Coordinator for more information, to register for a class or to schedule a private course.

Email: training@hardent.com
Telephone: 514-284-5252

Hardent

XILINX® | Authorized Training Provider